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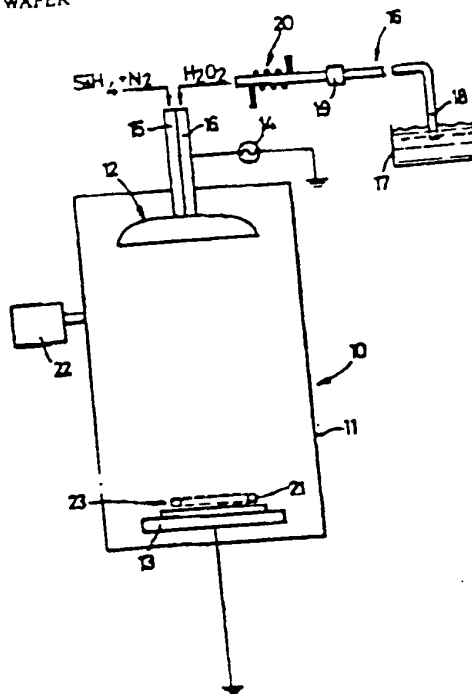
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(54) Title: A METHOD OF TREATING A SEMICONDUCTOR WAFER

(57) Abstract

This invention relates to a method of treating a semiconductor wafer and in particular, but not exclusively, to planarisation. The method consists of depositing a liquid short-chain polymer formed from a silicon containing gas or vapour. Subsequently water and OH are removed and the layer is stabilised.



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A method of treating a semi-conductor wafer

This invention relates to a method for treating a semi-conductor wafer and in particular, but not exclusively, to what is known as planarisation.

5 It is common practice in the semi-conductor industry to lay down layers of insulating material between conducting layers in order to prevent short circuits. If a layer of insulating material is simply deposited in the normal way undulations begin to build up as the layers pass over the
10 metallic conductors which they are designed to insulate. Various techniques have been developed to try to overcome this problem by filling the trenches or valleys between the conductors to a height above the top of the conductors so that after treatment a generally planar layer exists on the
15 top of the wafer. One example of such a technique is to spin on layers of polyimide to smooth out the surfaces. However, in practice, narrow trenches tend to be incompletely filled whilst wide valleys are not fully levelled. As the 2-D dimensions of devices are reduced,
20 these problems are accentuated.

From one aspect the invention consists in a method of treating a semi-conductor wafer comprising, depositing a liquid short-chain polymer having the general formula $\text{Si}_x(\text{OH})_y$ or $\text{Si}_x\text{H}_y(\text{OH})_z$ on the wafer to form a generally planar
25 layer.

The reference to the polymer being liquid is simply intended to indicate that it is neither gaseous nor

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solidified at the moment of deposition.

From one aspect the invention consists in a method of treating a semi-conductor wafer in a chamber including, introducing into the chamber a silicon-containing gas or vapour and a compound, containing peroxide bonding, in vapour form, reacting the silicon-containing gas or vapour with the compound to form a short-chain polymers and condensing the polymer on the wafer to form a generally planar layer.

10 The silicon-containing gas or vapour may be inorganic and preferably is silane or a higher silane, which may be introduced into the chamber with an inert carrier gas, for example nitrogen. The compound may be, for example, hydrogen peroxide or ethandiol.

15 The method may further comprise removing water and/or OH from the layer. For example the layer may be exposed to a reduced pressure and/or exposed to a low power density plasma, which may heat the layer to 40° to 120°C.

The method may further comprise forming or depositing an under layer prior to the deposition of the polymer. This under layer may be silicon dioxide and may have a thickness of between 1000 and 3000Å. It may for example be 2000Å thick. The under layer may conveniently be deposited by plasma enhanced chemically vapour deposition. Either the under layer and/or the wafer may be pre-treated by, for example a plasma, to removing contaminants. In that case it may be pretreated with a plasma, for example using oxygen as a reactive gas.

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Similarly the surface of the deposited polymer layer may be treated in a plasma using a reactive oxygen gas in order to enhance chain lengthening and cross-linking within the polymer. This gas could be, for example, oxygen, nitrogen or hydrogen peroxide vapour and other gases may be appropriate. The plasma has a heating effect which enhances crosslinking, but there may also be a radiation effect from the various gases. This chain linking may alternatively be catalysed by exposing the polymer layer to UV light, x-rays or ion bombardment. However, in many applications acceleration of chain linking may not be desirable; instead it may be desirable for the polymer molecule particles to settle before significant chain linking occurs.

The method may further comprise depositing or forming a capping layer on the surface of the deposited layer. This capping layer may be silicon dioxide. The capping layer is deposited after a proportion of the condensation reactions have occurred and water has been removed from the layer.

The method may further comprise heating the polymer layer and this heating preferably takes place after capping. The polymer layer may be heated to between 180-220°C for between 50-70 minutes. For example it may be heated to 220°C for 60 minutes. The layer may subsequently be allowed to cool to an ambient temperature and then reheated to 430-470°C for 30-50 minutes. For example the second heating may last 40 minutes at 450°C. Indeed this second heating may suffice and may be achieved using a furnace, heat lamps, a hotplate or plasma heating.

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In one preferred arrangement the polymer layer may be heated to between 200-450°C, prior to capping, in order that the cap can be deposited at elevated temperatures. Although the capping layer could be deposited in one or more steps e.g. a 'cold' capping layer deposited at the temperature of the planarising layer followed by a hot capping layer; the polymer layer having first been heated to 200-450°C as described above.

The density of the hydrogen peroxide may be in the range of 1.20-1.35 gms/cc and a density of 1.25 gms/cc may be particularly preferred. The hydrogen peroxide is preferably at 50% concentration when introduced into the chamber.

The ambient temperature within the chamber may be within the range of 0-80°C during the deposition of the polymer layer, but the wafer platten is preferably at 0°C or at the dew point of the polymer when in vapour form. Low pressure is also desirable but requires low temperatures (eg 400mT, -10°C).

In order to avoid heating the platten, the wafer is preferably lifted from the platten for each processing step which involves heating.

The method can be used to achieve planarisation or gap filling. In the latter case the ambient chamber temperature may conveniently be even higher.

The invention also includes wafers treated by any of the methods set out above and semi-conductor devices including polymer layers formed by the method above.

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The invention may be performed in various ways and a specific embodiment will now be described, by way of example, with reference to the following drawings, in which;

Figure 1 is a schematic view for apparatus for performing the treatment method;

Figures 2A and 2B are hugely magnified photographs of cross-sections of a wafer treated by the method; and

Figures 3A to E illustrate schematically the steps of the process.

Apparatus for treating semi-conductor wafers is schematically illustrated at 10 in Figure 1. It will be understood that only the features which are particularly required for the understanding of the invention are described and illustrated. The general construction of such apparatus is well known in the art.

Thus, the apparatus 10 includes a chamber 11 having a duplex shower head 12 and a wafer support 13. The shower head 12 is connected to RF source 14 to form one electrode, whilst the support 13 is earthed and forms another electrode. Alternatively the R.F. source 14 could be connected to the support 13 and the shower head 12 earthed. The shower head 12 is connected by respective pipes 15 and 16 to a source of SiH_4 in N_2 or other inert carrier and a source 16 of H_2O_2 . The carrier gas is conveniently used for ease of operation of the equipment; it is believed that the process could be performed without it.

The source 16 comprises a reservoir 17 of H_2O_2 , an outlet pipe 18, a pump 19 and a flash heater 20 for

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vaporising the H_2O_2 .

In use the apparatus is arranged to deposit a short chain, inorganic polymer, which is initially a liquid, between the interconnects on a semi-conductor chip to produce planarisation either locally or globally, or for 'gap filling'. The polymer is formed by introducing into the chamber the silane and the hydrogen peroxide in vapour form and reacting them within the chamber spontaneously. Once the resultant polymer is deposited on the wafer, it has been found that its viscosity is such that it fills both small and large geometries or gaps and is generally self levelling. It is believed that effectively there is a settlement process taking place as the polymerisation takes place. The more settlement which occurs prior to full polymerisation the less likelihood there is of cracking. Very small dimensioned gaps can be filled and because of the fill layer properties these gaps can even, in certain circumstances, be re-entrant.

As has been mentioned, if left, the chains within the polymer will slowly extend and cross link. In some circumstances it may be desirable to accelerate this process by plasma treatment. This treatment produces UV radiation and it is believed that it is this radiation which is responsible for increasing the speed of chain extension and cross linking. Other forms of radiation treatment may therefore be equally applicable. A variety of gases may be appropriate for use at this stage, for example any inert gas or hydrogen, nitrogen or oxygen containing gases.

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For good quality films it is desirable to remove as much water and OH from the film at an early stage. This can be done by exposing the layer to a reduced pressure causing the layer to pump water out and the subsequently heating the
5 layer to between say 40°C and 120°C. A pump 22 is provided for reducing chamber pressure.

However in order to solidify fully the polymer layer, it has been found that it is generally necessary to subject the layer to more intense heat treatment. In many instances
10 it is necessary or desirable first to deposit a capping layer over the polymer. It is believed that this assists in providing mechanical stability for the polymer layer during cross linking. It may also help to control the rate at which the layer loses water during heating and so have a
15 controlling affect on shrinkage and cracking.

A suitable capping layer would be silicon dioxide.

The heat treatment stage after the capping involves removing excess water from the layer which is a by-product of the cross-linking reaction. The bake also removes SiOH
20 bonds. The speed at which the water is removed may be important and several ways of removing water have been successful. One suitable sequence comprises baking the layer for 60 minutes at 200°C, cooling it to ambient temperature and then rebaking it for 40 minutes at 450°C.
25 Microwave heating has also been successful. A simple bake at 450° will often also suffice, or the bakes may be replaced by the following steps:

1. 2000 Å 'cold' cap deposited at between 20-40°C.

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2. Plasma heat treatment in N_2O which raises the temperature to 300-400°C.

3. 4000-6000Å 'hot' cap is deposited.

Alternatively, in some cases, a single stage 'hot cap' deposited at 300-400°C will suffice.

It has been found that the adhesion of the polymer layer to the underlying substrate material can be enhanced by depositing an under layer, for example of silicon dioxide. Typically this should be of the order of 2000Å thickness and it may be laid down by plasma-enhanced chemical vapour deposition.

Examples of actual deposited layers are illustrated in the photographs of Figures 2A and 2B. It will be seen that the upper surface of the layers 21 are generally planar despite the huge magnification involved.

Although SiH_4 has proved to be particularly successful, it is believed that the method will be applicable with most silicon-containing gases or vapours. It has been found that to some extent a suitable polymer can be obtained with any concentration or density of H_2O_2 , but a density range 1.20-1.35 gms/cc has been particularly successful. The most preferred H_2O_2 density is 1.25 gms/cc. An H_2O_2 concentration of 50% is very effective but it is believed that the preferred concentration may vary depending on whether the object is to achieve planarisation or gap filling. It is preferred that more H_2O_2 is supplied than SiH_4 and it is particularly preferred that the $H_2O_2:SiH_4$ ratio is of the order of 3:1.

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In the event that the wafer needs to be removed from the chamber between processing stages, it may be desirable to pre-treat the exposed surface, when the wafer is placed back in the chamber, in order to remove any organics or other contaminants from the exposed surface.

Figures 3A to E illustrate the preferred processing sequence schematically and indicate the probable chemistry. It may be advantageous to wash the chamber with H_2O_2 between at least some of the processing stages.

As it is desirable to keep the platten or support 13 at around 0°C, the wafer may be lifted above the support 13 for each heating process so that the heat of the wafer is not significantly transmitted to the support 13. This can be achieved by arranging an intermediate position 23 for a wafer loading device 21.

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Claims

1. A method of treating a semi-conductor wafer comprising, depositing a liquid short-chain polymer having the general formula $\text{Si}_x(\text{OH})_y$ or $\text{Si}_x\text{H}_y(\text{OH})_z$ on the wafer to
5 form a generally planar layer.
2. A method of treating a semi-conductor wafer, including positioning the wafer in a chamber, introducing into the chamber silicon-containing gas or vapour and a compound, containing peroxide bonding, in vapour form,
10 reacting the silicon-containing gas or vapour with the compound to form a short-chain polymer and condensing the polymer on the wafer to form a generally planar layer.
3. A method as claimed in Claim 2 wherein the silicon-containing gas or vapour is a silane or higher
15 silane.
4. A method as claimed in Claim 2 or Claim 3 wherein the compound is hydrogen peroxide or ethandiol.
5. A method as claimed in any one of the preceding claims further comprising removing water and/or OH from the
20 layer.
6. A method as claimed in Claim 5 wherein the water and/or OH removing step includes exposing the layer to a reduced pressure.
7. A method as claimed in Claim 6 wherein the layer
25 is exposed to reduced pressure for between 1.5 and 2.5 minutes.
8. A method as claimed in any one of the Claims 5 to

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7 wherein water and/or OH removing step includes exposing the layer to a low power density plasma.

9. A method as claimed in Claim 8 wherein the plasma heats the layer to between 40° to 120°C.

5 10. A method as claimed in any one of the preceding claims further comprising forming or depositing an under layer prior to the deposition of the polymer layer.

11. A method as claimed in Claim 10 wherein the under layer is deposited by chemical vapour deposition.

10 12. A method as claimed in Claim 11 wherein the wafer is preheated prior to the under layer deposition.

13. A method as claimed in any one of the preceding claims further comprising depositing a capping layer on the polymer layer after substantially all the water has been
15 removed from the polymer layer.

14. A method as claimed in Claim 13 wherein the capping layer is SiO₂.

15. A method as claimed in Claim 13 or Claim 14 including heat treating the wafer after the capping layer
20 has been deposited.

16. A method as claimed in any one of the preceding Claims wherein the wafer is located on a platten maintained at or below the dew point of the silicon-containing vapour.

17. A method as claimed in Claim 16 wherein the wafer
25 is lifted from platten for any processing step involving or causing heating of the wafer.

18. A method as claimed in Claim 17 wherein the lifted position lies between the platten and a wafer load/unloaded

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position.

19. A method as claimed in Claim 4 and Claims 5 to 18 as dependent on Claim 4 wherein the compound is hydrogen peroxide of between 45% and 55% concentration.

5 20. A method as claimed in Claim 19 wherein the concentration of the hydrogen peroxide is 50%.

21. A method as claimed in any one of Claims 2 to 20 on Claim 4 wherein the silicon-containing gas or vapour and the compound are reacted in a chemical vapour deposition
10 process.

22. A method as claimed in Claim 21 wherein the reaction takes place between electrodes and wherein the silicon-containing gas or vapour and the compound are kept apart until they are introduced between the electrodes.

15 23. A method as claimed in any one of the preceding Claims wherein the gas is SiH_4 and the compound is H_2O_2 and there is more H_2O_2 than SiH_4 .

24. A method as claimed in Claim 23 wherein the $\text{H}_2\text{O}_2:\text{SiH}_4$ ratio is of the order of 3:1.

20 25. A method as claimed in any one of the preceding Claims wherein the chamber is washed through with the compound between at least two processing steps.

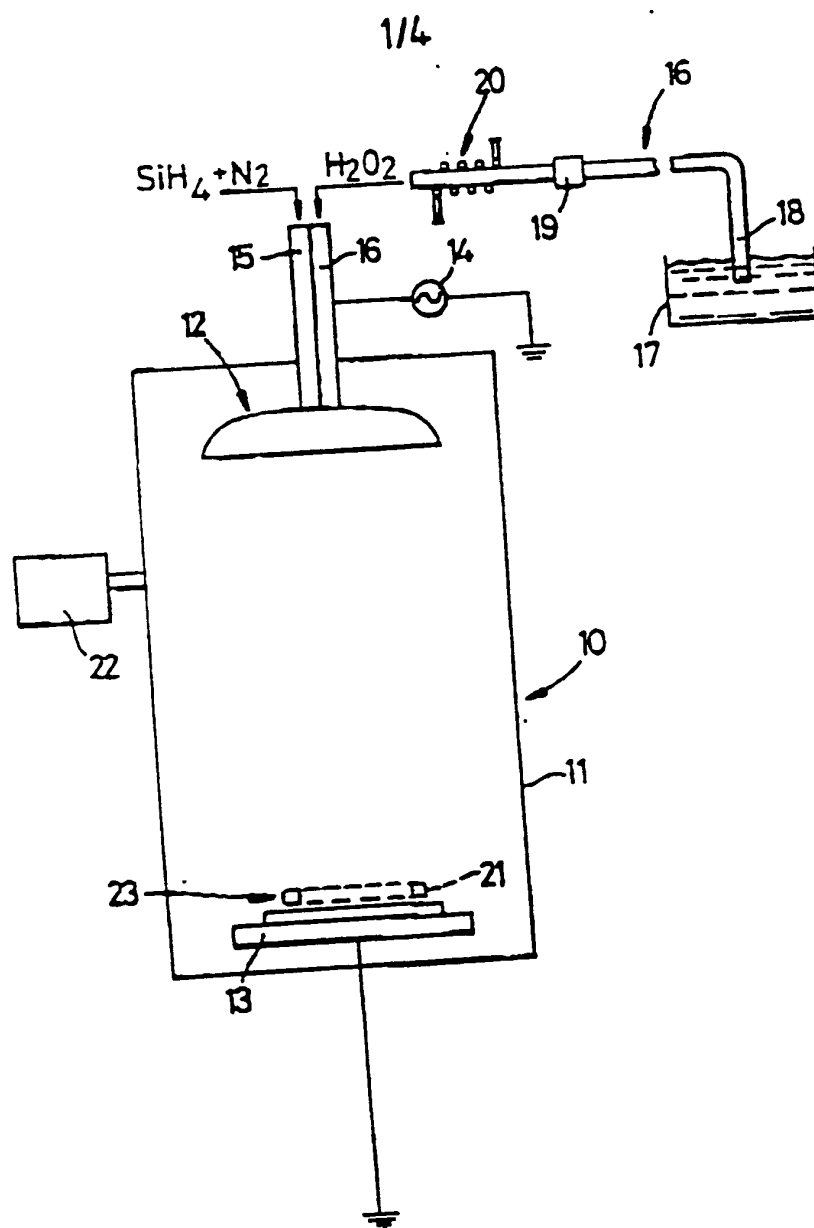
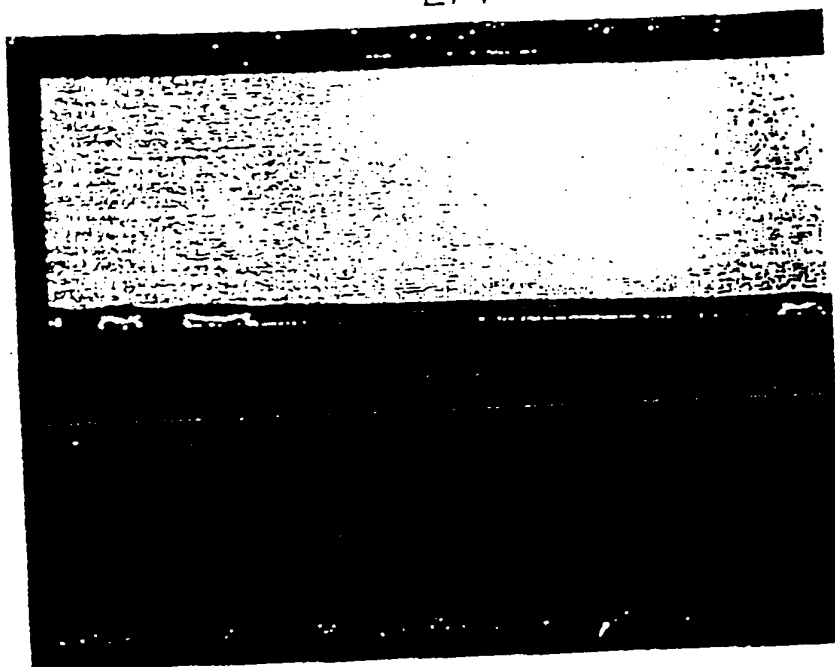


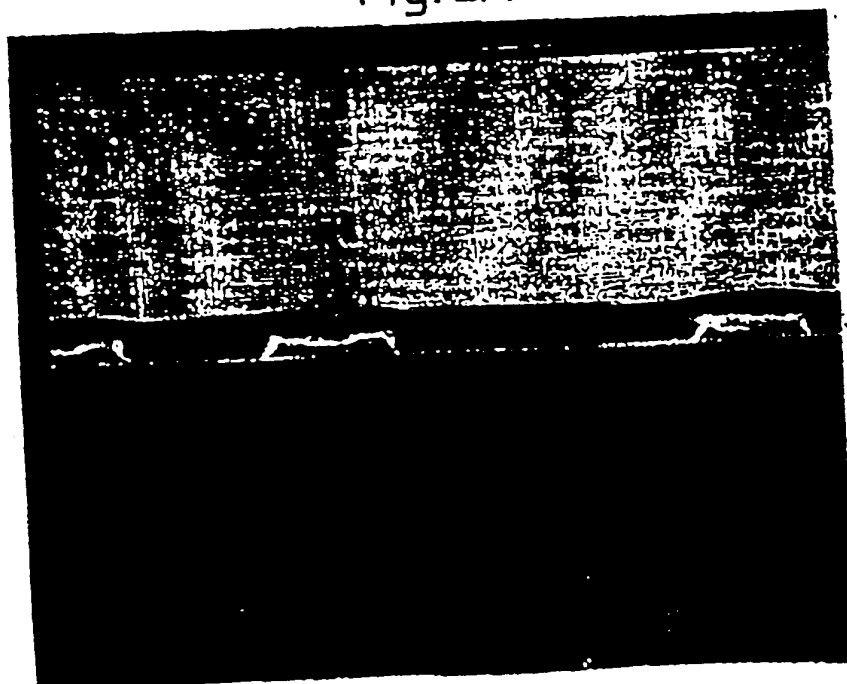
Fig.1

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Fig. 2A

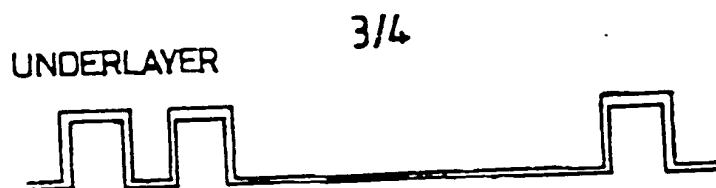


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Fig. 2B

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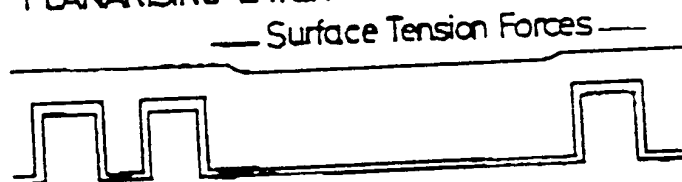
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PECVD
300 Deg C
Adhesion Enhancer
 $\text{SiH}_4 + 2\text{N}_2\text{O} \rightarrow \text{SiO}_2 \downarrow + 2\text{H}_2 + 2\text{N}_2$

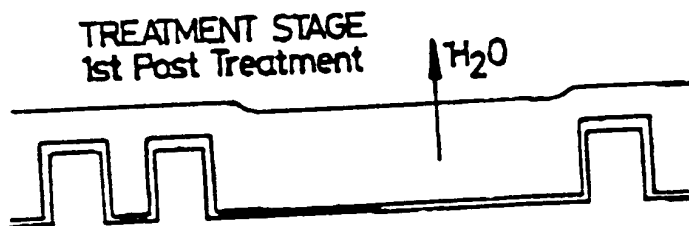
Fig. 3A

PLANARISING LAYER



CVD
Approx. 0 Deg C
Planarises features
 $\text{SiH}_4 + 3\text{H}_2\text{O}_2 \rightarrow \text{Si(OH)}_4 \downarrow + 2\text{H}_2\text{O} + \text{H}_2$

Fig. 3B



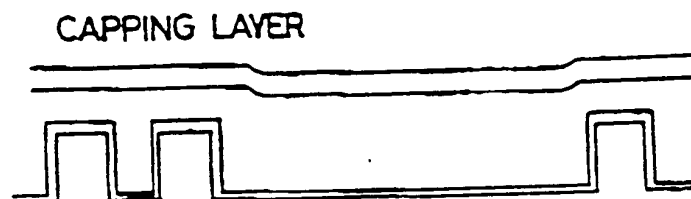
Pumpout at approx. 0 Deg C
Pumpout at approx. 150 Deg C
Promotion of Polymerisation
Removal of water
 $\text{Si(OH)}_4 \rightarrow \text{SiO}_2 + 2\text{H}_2\text{O} \uparrow$

Fig. 3C

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PECVD
300 DEG C

Provides mechanical stability
during densification step

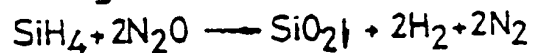
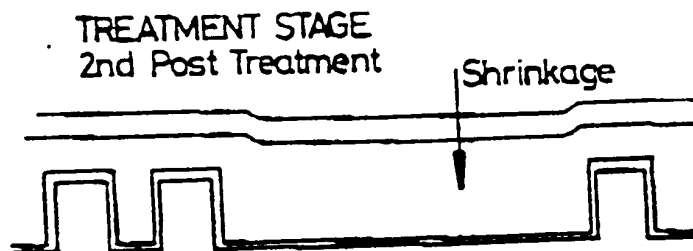


Fig. 3D



Anneal at 450 Deg C
Densification of film

Furnace
Heat Lamps
Hot Plate
Plasma

Fig. 3E

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INTERNATIONAL SEARCH REPORT

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I. CLASSIFICATION OF SUBJECT MATTER <small>(Of several classification symbols apply, indicate all)*</small> According to International Patent Classification (IPC) or to both National Classification and IPC Int.Cl. 5 H01L21/316; C23C16/56	
II. FIELDS SEARCHED Minimum Documentation Searched? Classification System Int.Cl. 5 H01L : C23C	
Documentation Searched other than Minimum Documentation to the Extent that such Documents are included in the Fields Searched	
III. DOCUMENTS CONSIDERED TO BE RELEVANT*	
Category* A A A	Citation of Document, U. with indication, where appropriate, of the relevant passages PATENT ABSTRACTS OF JAPAN vol. 8, no. 155 (E-256)(1592) 19 July 1984 & JP,A,59 57 437 (FUJITSU K.K.) 3 April 1984 see abstract --- PATENT ABSTRACTS OF JAPAN vol. 11, no. 101 (C-413)31 March 1987 & JP,A,61 250 032 (HITACHI CHEM CO LTD) 7 November 1986 see abstract --- PATENT ABSTRACTS OF JAPAN vol. 15, no. 046 (E-1029)4 February 1991 & JP,A,22 78 850 (FUJI ELECTRIC CO LTD) 4 February 1991 see abstract --- -/-
Relevance to Claim No.13 1 1 1,5, 10-11, 13-14	
* Special categories of cited documents : "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document not published on or after the international filing date "L" document which may throw doubts on priority claims or which is used to establish the publication date of another document or other special reason (as specified) "U" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is considered with one or more other such documents, such combination being obvious to a person skilled in the art. "A" document member of the same patent family	
IV. CERTIFICATION Date of the Annual Completion of the International Search 24 AUGUST 1993	
Date of Mailing of this International Search Report 08.09.93	
International Searching Agency EUROPEAN PATENT OFFICE	
Signature of Authorized Officer SCHUERMANS N.F.	

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RE DOCUMENTS CONSIDERED TO BE RELEVANT		International Application No.
(CONTINUED FROM THE SECOND SHEET)		
Category *	Classification of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No.
A	<p>DATABASE WPI Section Ch. Week 2588, 16 May 1988 Derwent Publications Ltd., London, GB; Class J, AN 88-172055 & JP.A, 63 110 642 (SEIKO EPSON K.K.) 16 May 1988 see abstract</p>	2-4
A	<p>US, A, 4 812 325 (SHUNICHI I. ET AL.) 14 March 1989 see column 2, line 55 - line 59 see claim 1</p>	2-4

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**ANNEX TO THE INTERNATIONAL SEARCH REPORT
ON INTERNATIONAL PATENT APPLICATION NO.**GB 9301368
SA 75943

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report.
The members are as contained in the European Patent Office EDP file on
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Patent document cited in search report	Publication date	Patent family number(s)	Publication date
US-A-4812325	14-03-89	JP-A- 62096674 JP-A- 62099464	06-05-87 08-05-87

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/83